# HIT מכון טכנולוגי חולון – ויקיפדיה t

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# VHDLמעבדה ל

# רמזור

# מגישים : רפאל איבגי - 316363449

# חיים עוזר -316063569

# Design:

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**STD\_LOGIC\_UNSIGNED**.ALL;**

**entity** ramzor **is**

**port** **(**

TEST**,**STBY**,**CLOCK**:** **in** STD\_LOGIC**;**

r1**,**y1**,**g1**,**r2**,**g2**,**y2**:** **buffer** STD\_LOGIC**);**

**end;**

**architecture** arc **of** ramzor **is**

**component** Signal\_Gen **port** **(**

clk**:** **in** STD\_LOGIC**;**

mode**:** **in** STD\_LOGIC**;**

result**:** **out** std\_logic**);**

**end** **component;**

**component** SMramzor **port** **(**

clk**,** stby**:** **IN** std\_logic**;**

r1**,**y1**,**g1**,**r2**,**g2**,**y2 **:** **OUT** std\_logic **);**

**end** **component;**

**signal** clk1 **:** std\_logic**;**

**signal** A**:**std\_logic**;**

**begin**

clkO**:** signal\_gen **port** **map(**CLOCK**,**A**,**clk1**);**

sm**:** SMramzor **port** **map(**STBY**,**clk1**,**r1**,**y1**,**g1**,**r2**,**g2**,**y2**);**

**process(**clock**)**

**begin**

**if** TEST**=**'1' **then**

A**<=**'0'**;**

**else** A**<=**'1'**;** **end** **if;**

**end** **process;**

**end;**

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

**entity** Signal\_Gen **is**

**port** **(**

clk**:** **in** STD\_LOGIC**;**

mode**:** **in** STD\_LOGIC**;**

result**:** **out** std\_logic**);**

**end;**

**architecture** reg **of** Signal\_Gen **is**

**signal** y**:** std\_logic**:=** '0'**;**

**signal** counter**:** integer **:=**0**;**

**begin**

**process** **(**clk**)**

**begin**

**if** **falling\_edge(**clk**)** **then**

counter**<=** counter**+**1**;**

**case** mode **is**

**when** '0' **=>**

**if** **(**counter **>** 50000000**)** **then** counter **<=**0**;**

**elsif** counter**=**25000000 **then** y**<=**'1'**;**

**else** y**<=**'0'**;** **end** **if;**

**when** **others** **=>**

**if** **(**counter **>** 50000000**\***5**)** **then** counter **<=**0**;**

**elsif** counter **=** 125000000 **then** y**<=**'1'**;**

**else** y**<=**'0'**;** **end** **if;**

**end** **case;** **end** **if;**

result**<=**y**;**

**end** **process;**

**end** reg**;**

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**STD\_LOGIC\_UNSIGNED**.ALL;**

**entity** SMramzor **is** **port** **(**

clk**,** stby**:** **IN** std\_logic**;**

r1**,**y1**,**g1**,**r2**,**g2**,**y2 **:** **OUT** std\_logic **);**

**end;**

**architecture** arc **of** SMramzor **is**

**Type** stat\_typ **is** **(**YY**,**RY**,** GR**,** YR**,** RG**);**

**Signal** cur\_state**,** next\_state**:**stat\_typ**;**

**Begin**

**Process(**clk**)**

**Begin**

**if** **(**stby **=**'1'**)** **then**

r1 **<=**'0'**;** r2**<=**'0'**;** y1**<=**'1'**;** y2**<=**'1'**;** g1**<=**'0'**;** g2**<=**'0'**;**

**elsif** **falling\_edge(**clk**)** **then**

**Case** cur\_state **is**

**When** YY **=>** r1**<=**'0'**;** r2**<=**'0'**;** y1**<=**'1'**;** y2**<=**'1'**;** g1**<=**'0'**;** g2**<=**'0'**;**

next\_state **<=**RY**;**

**When** RG **=>** r1**<=**'1'**;** r2**<=**'0'**;** y1**<=**'0'**;** y2**<=**'0'**;** g1**<=**'0'**;** g2**<=**'1'**;**

next\_state **<=** RY**;**

**When** RY **=>** r1**<=**'1'**;** r2**<=**'0'**;** y1**<=**'0'**;** y2**<=**'1'**;** g1**<=**'0'**;** g2**<=**'0'**;**

next\_state **<=**GR**;**

**When** GR **=>** r1**<=**'0'**;** r2**<=**'1'**;** y1**<=**'0'**;** y2**<=**'0'**;** g1**<=**'1'**;** g2**<=**'0'**;**

next\_state **<=**YR**;**

**When** YR **=>** r1**<=**'0'**;** r2**<=**'1'**;** y1**<=**'1'**;** y2**<=**'0'**;** g1**<=**'0'**;** g2**<=**'0'**;**

next\_state **<=** RG**;**

when others => r1<='0'; r2<='0'; y1<='0'; y2<='0'; g1<='0'; g2<='0';

next\_state <= YY;

End case;

end if;

End process;

End;

Top Level:

**library** ieee**;**

**Use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

**entity** TopRamzor **is** **port** **(**

CLOCK50\_**:** **in** STD\_LOGIC**;**

sw**:** **in** STD\_LOGIC\_VECTOR**(**1 **downto** 0**);**

ledr**:** **out** STD\_LOGIC\_VECTOR**(**5 **downto** 0**)**

**);**

**end;**

**architecture** arc **of** TopRamzor **is**

**component** ramzor **is** **port** **(**

TEST**,**STBY**,**CLOCK**:** **in** STD\_LOGIC**;**

r1**,**y1**,**g1**,**r2**,**g2**,**y2**:** **buffer** STD\_LOGIC**);**

**end** **component;**

**begin**

Total**:** ramzor **port** **map(**

sw**(**0**),**sw**(**1**),**CLOCK50\_**,** ledr**(**0**),** ledr**(**1**),** ledr**(**2**),** ledr**(**3**),** ledr**(**5**),** ledr**(**4**));**

**end;**

RTL:





